AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

2. (Previously Presented) A semiconductor integrated circuit device comprising:

a conductive connecting member;

a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and an alloy layer is provided having the melting point higher than that of a solder having Pb as a main composition metal, wherein said alloy layer contains no Pd as a main composing metal and substantially no Pb; and

a resin molding said connected first portion,

wherein said alloy layer is provided at a second portion of said connected member outside of said resin.

3. (Previously Presented) A semiconductor integrated circuit device comprising:

a conductive connecting member;

a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and a metal layer is provided having the melting point higher than that of an Sn-Pb eutectic

solder, wherein said metal layer contains no Pd as a main composing metal and substantially no Pb; and

a resin molding said connected first portion,

wherein said metal layer is provided at a second portion of said connected member outside of said resin.

4. (Currently Amended) A semiconductor integrated circuit device comprising:

a conductive connecting member;

a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and a Pb-free metal layer, having the melting point higher than Sn-Pb eutectic solder, wherein said Pb-free metal layer contains no Pd as a main composing metal; and

a resin molding said connected first portion,

wherein said Pb-free metal layer is provided at a second portion of said connected member outside of said resin.

5. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor chip;

a conductive connecting member connected to said semiconductor chip;

a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and a Pb-free metal layer having the melting point higher than that of an Sn-Pb eutectic solder,

wherein said Pb-free metal layer contains no Pd as a main composing metal, wherein said Pb-free metal layer is provided in a second portion of the connected member other than said first portion; and

a resin molding said semiconductor chip connected to said connecting portion, said connecting member and said first portion of said connected portion to which said connecting member is connected.

6. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire bonded to said semiconductor chip;

a lead including an inner lead portion and an outer lead portion, wherein a metal layer including a palladium layer is plated on said inner lead portion and is bonded to said wire, and wherein a Pb-free alternate solder, having the melting point higher than that of an Sn-Pb eutectic solder, and which Pb-free alternate solder contains no Pd as a main composing metal, is plated on a mounted portion of said outer lead portion; and

a resin molding a bonding portion of said semiconductor chip to which said wire is bonded, said wire and the inner lead portion of said lead to which said wire is bonded.

7. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire;

a resin molding said semiconductor chip and

said wire; and

a lead in which a metal layer including a palladium layer is provided in a front end portion of said lead molded by said resin, and a Pb-free metal layer, having the melting point higher than an Sn-Pb eutectic solder, which Pb-free metal layer contains no Pd as a main composing metal, is provided at an outer portion of said lead which is not molded by said resin.

8. (Canceled)

9. (Previously Presented) A mounting substrate structure comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a conductive connecting member, a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and an alloy containing no Pd as a main composing metal and substantially no Pb is provided in a second portion of said connected member, and a resin molding said first portion of said connected member to be connected; and

a printed circuit board,

wherein said semiconductor integrated circuit device is connected to said printed circuit board by a solder having the melting point higher than that of a solder having Pb as a main composing metal and

wherein said second portion of said connected member is outside of said resin.

10. (Previously Presented) A mounting substrate structure comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a conductive connecting member, a connected member in which a metal layer including a palladium layer is provided at a first portion to which said connecting member is connected, and a metal containing no Pd as a main composing metal and substantially no Pb at a second portion, and a resin molding said first portion of said connected member to be connected to said connecting member; and

a printed circuit board to which said semiconductor integrated circuit device is connected by a metal having the melting point higher than that of a solder having Pb as a main composing metal,

wherein said second portion of said connected member is outside of said resin.

11. – 17. (Canceled)

18. (Previously Presented) A semiconductor integrated circuit device according to claim 2, wherein said palladium layer is not provided at said second portion of the connected member outside of the resin.

19. (Previously Presented) A semiconductor integrated circuit device according to claim 3, wherein said palladium layer is not provided at said second portion of the connected member outside of the resin.

20. (Previously Presented) A semiconductor integrated circuit device according to claim 4, wherein said palladium layer is not provided at said second portion of the connected member outside of the resin.

21. (Previously Presented) A semiconductor integrated circuit device according to claim 5, wherein said palladium layer is not provided at said second portion of the connected member.

22. (Previously Presented) A semiconductor integrated circuit device according to claim 6, wherein said palladium layer is not provided at said outer lead portion of said lead.

23. (Previously Presented) A semiconductor integrated circuit device according to claim 7, wherein said palladium layer is not provided at said second portion of the connected member.

24. (Previously Presented) A mounting substrate structure according to claim 9, wherein said palladium layer is not provided at said second portion of the connected member outside of the resin.

25. (Previously Presented) A mounting substrate structure according to claim 10, wherein said palladium layer is not provided at said second portion of the connected member outside of the resin.